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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	MI22-1384
First Inventor or Application Identifier	Moore
Title	Methods of Forming Oxide Regions Over...
Express Mail Label No.	EL466558402

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
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1. [XX] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)
2. [XX] Specification [Total Pages 24] (plus cover pg.)
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [XX] Drawing(s) (35 U.S.C. 113) [Total Sheets 4]
4. Oath or Declaration [Total Pages 2]
   a. [XX] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below]
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
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ACCOMPANYING APPLICATION PARTS

8. [XX] Assignment Papers (cover sheet & document(s))
9. [XX] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [XX] Power of Attorney
10. [ ] English Translation Document (if applicable)
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [XX] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
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* A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:
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Prior application information: Examiner ______ Group / Art Unit: ______

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Signature	[signature]	Date	6/22/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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Methods of Forming Oxide Regions Over Semiconductor Substrates, and Methods of Forming Transistors Associated With Semiconductor Substrates

* * * * *

INVENTORS

John T. Moore

ATTORNEY'S DOCKET NO. MI22-1384

Methods of Forming Oxide Regions Over Semiconductor Substrates, and Methods of Forming Transistors Associated With Semiconductor Substrates

TECHNICAL FIELD

The invention pertains to methods of forming oxide regions over semiconductor substrates, and in particular embodiments pertains to methods of forming two or more transistors associated with a semiconductor substrate.

BACKGROUND OF THE INVENTION

Oxide regions, such as, for example, silicon dioxide regions, have numerous applications in semiconductor devices. For instance, a thin layer of silicon dioxide is frequently placed between the conductive material of a transistor gate and an underlying semiconductor substrate, with such layer of silicon dioxide frequently being referred to as so-called "gate oxide". The thickness of the gate oxide can affect various electrical properties of a transistor structure incorporating the gate oxide, and accordingly it is desired to control the gate oxide thickness during device fabrication.

Transistor devices which are commonly used in semiconductor assemblies are PMOS transistor devices and NMOS transistor devices. Each type of transistor device has particular electrical properties associated therewith, and accordingly there can be advantages in utilizing

different gate oxide structures for some of the transistor devices associated with a semiconductor structure relative to others of the transistor devices associated with a semiconductor structure.

In light of the importance of gate oxide structures in semiconductor device fabrication, it is desired to develop new methods for forming oxide regions associated with semiconductor structures.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming an oxide region over a semiconductor substrate. A nitrogen-containing layer is formed across at least some of the substrate. After the nitrogen-containing layer is formed, an oxide region is grown from at least some of the substrate. The nitrogen of the nitrogen-containing layer is dispersed within the oxide region.

In another aspect, the invention encompasses a method of forming a pair of transistors associated with a semiconductor substrate. A substrate is provided. A first region of the substrate is defined, and additionally a second region of the substrate is defined. The first region is a p-type doped region, and the second region is an n-type doped region. A first oxide region is formed which covers at least some of the first region of the substrate, and which does not cover any of the second region of the substrate. A nitrogen-comprising layer is formed across at least some of the first oxide region and across at least some of the

second region of the substrate. After the nitrogen-comprising layer is formed, a second oxide region is grown from the second region of the substrate. A first transistor gate is formed over the first oxide region, and a second transistor gate is formed over the second oxide region. First source/drain regions are formed proximate the first transistor gate to form a PMOS transistor comprising the first transistor gate. Second source/drain regions are formed proximate the second transistor gate to form an NMOS transistor comprising the second transistor gate.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, cross-sectional view of fragments of a semiconductor wafer shown at a preliminary processing step of the present invention.

Fig. 2 is a view of the Fig. 1 fragments shown at a processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragments shown at a processing step subsequent to that of Fig. 5.

Fig. 7 is a diagrammatic, schematic, cross-sectional view of an exemplary remote plasma nitridation apparatus which can be utilized in methodology of the present invention.

Fig. 8 is a diagrammatic, cross-sectional view of another apparatus which can be utilized in methodology of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

A semiconductor wafer 10 is shown in fragmentary view in Fig. 1, and specifically is shown to comprise a first fragmentary region 12 and a second fragmentary region 14. Wafer 10 comprises a substrate 16. Substrate 16 can, for example, comprise a bulk semiconductive material, such as, for example, monocrystalline silicon lightly doped with a background p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive

material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Regions 12 and 14 can correspond to differently-doped regions of substrate 16. For instance, region 12 can correspond to a portion of substrate 16 having a heavier concentration of n-type conductivity enhancing dopant than p-type conductivity enhancing dopant, and can accordingly be referred to as an n-type doped region. Further, region 14 can correspond to a region of substrate 16 wherein the p-type dopant concentration is heavier than any n-type dopant concentration, and can accordingly be referred to as a p-type region of substrate 10. In order to emphasize this aspect of the invention and assist in the description that follows, substrate 16 of region 12 is labeled with an "n", and region 14 is labeled with a "p". It is to be understood that the shown doping of regions 12 and 14 corresponds to a particular embodiment of the present invention, and that other embodiments are encompassed wherein both of regions 12 and 14 are similarly doped, including embodiments wherein regions 12 and 14 are both heavier doped with n-type dopant than p-type dopant, as well as embodiments wherein regions 12 and 14 are both heavier doped with p-type dopant than n-type dopant.

In particular embodiments of the present invention, regions 12 and 14 correspond to portions of a semiconductor memory assembly, and in such embodiments regions 12 and 14 can both correspond to memory

array regions, or can both correspond to regions peripheral to a memory array region, or alternatively one of regions 12 and 14 can correspond to a memory array region while the other regions 12 and 14 corresponds to a portion of the wafer peripheral to the memory array region.

Referring to Fig. 2, an oxide layer 18 is formed over substrate 16. Oxide 18 is shown formed over both of regions 12 and 14. Oxide layer 18 can comprise, for example, silicon dioxide, and can be formed by, for example, chemical vapor deposition over substrate 16. Alternatively, oxide layer 18 can be formed by exposing substrate 16 to oxidizing conditions. For instance, if substrate 16 comprises monocrystalline silicon, a silicon dioxide layer 18 can be formed by oxidizing a surface of substrate 16. Oxide layer 18 is preferably formed to a thickness of less than 70Å, and can be formed to a thickness of less than or equal to about 50Å, such as, for example, a thickness of about 30Å.

A patterned masking layer 20 is shown formed over oxide layer 18 to mask the portion of oxide layer 18 in region 12, while leaving the portion of oxide layer 18 of region 14 exposed. Masking layer 20 can comprise, for example, photoresist, and can be patterned by photolithographic processing. Although masking layer 20 is shown covering an entirety of oxide 18 of region 12, and not covering any of oxide 18 of region 14, it is to be understood that the invention encompasses other embodiments wherein masking layer 20 covers only a

portion of oxide 18 over region 12, and further encompasses embodiments wherein masking layer 20 also covers a portion of oxide layer 18 of region 14.

Referring to Fig. 3, the exposed portion of oxide 18 of region 14 is removed. Such can be accomplished by, for example, exposing wafer 10 to hydrofluoric acid. Masking layer 20 (Fig. 2) protects oxide 18 from being exposed to the oxide-removing etchant, and accordingly oxide 18 remains over region 12 after removal of oxide 18 from region 14.

It is to be understood that the processing of Figs. 2 and 3 is but one exemplary method of forming the structure shown in Fig. 3, and that other methods are encompassed by the present invention. In any event, the structure corresponding to Fig. 3 is preferably ultimately formed, with such structure having oxide 18 covering at least some of region 12 of substrate 16, and not covering at least some of region 14 of substrate 16.

Referring to Fig. 4, a nitrogen-comprising layer 22 is formed over regions 12 and 14. More specifically, nitrogen-comprising layer 22 is formed on and/or within at least some of oxide layer 18 of region 12, and further is formed on and/or within at least some of substrate 16 of region 14. Nitrogen-comprising layer 22 is preferably kept within a surface region of oxide 18 of region 12, and also within a surface region of substrate 16 of region 14. For purposes of interpreting this disclosure

and the claims that follow, a surface region is defined to be a region which extends to no more than 10Å beneath a surface, and in particular embodiments nitrogen-comprising region 22 extends no more than 5Å beneath an upper surface of either substrate 16 of region 14 or oxide 18 of region 12.

Nitrogen-comprising region 22 can be formed by, for example, remote plasma nitridization utilizing, for example, an apparatus 200 described with reference to Fig. 7. Apparatus 200 comprises a plasma chamber 202 and a reaction chamber 204. Reaction chamber 204 comprises a substrate holder 206, and substrate 16 is supported within chamber 204 by holder 206. Preferably, holder 206 is configured to rotate substrate 16 during exposure of substrate 16 to activated nitrogen species. Such activated nitrogen species are formed within plasma chamber 202 by, for example, exposing N_2 and/or other nitrogen-containing materials (for example, N_2O and/or NH_3) to plasma conditions, with the term "activated" indicating that the nitrogen species is different than the form of nitrogen fed to the plasma. An activated nitrogen species can comprise, for example, a nitrogen ion or a nitrogen atom in an energy state higher than its ground state. Exemplary plasma conditions comprise utilization of a microwave plasma generator at a power of from about 1,500 watts to about 3,000 watts, and a pressure within chamber 202 of less than or equal to about 3 Torr.

The plasma of chamber 202 forms activated nitrogen species which migrate along a passageway 208 into chamber 204 whereupon the species can form nitrogen-comprising layer 22 (Fig. 4) over substrate 16. An arrow is shown within passageway 208 to indicate migration of plasma activated nitrogen species through passageway 208.

Preferably, passageway 208 is of sufficient length so that plasma 202 is at least about 12 inches from substrate 16. Such can enable highly activated nitrogen species formed within a plasma to relax prior to interaction with substrate 16, which can limit penetration of the nitrogen species into substrate 16 relative to an amount of penetration which would occur with more highly activated species. In order to further limit penetration of nitrogen species into substrate 16, substrate 16 is preferably not biased relative to the plasma within chamber 202.

Suitable operating conditions for forming a nitrogen-comprising plasma over substrate 16 can include maintaining a temperature of substrate 16 at from about 550°C to about 1,000°C, rotating the wafer at about 90 rotations per minute (RPM), maintaining a pressure within chambers 202 and 204 of from about 0.8 Torr to about 2.8 Torr, and exposing the wafer to the nitridization conditions for a time of from about one minute to about five minutes.

An alternative apparatus which can be utilized for forming nitrogen-comprising layer 22 (Fig. 4) is described with reference to Fig. 8

as apparatus 220. Apparatus 220 can be referred to as a high density plasma remote plasma nitridization (HDP-RPN) apparatus, or simply as a plasma nitridization (PN) apparatus. Apparatus 220 comprises a reaction chamber 222 having a wafer holder 224 therein. Wafer 16 is supported on holder 224. A plasma 226 is formed above substrate 16, and preferably is maintained a distance "X" from substrate 16, with distance "X" corresponding to at least about four inches. Nitrogen is introduced into plasma 226 in the form of, for example, N_2, and activated nitrogen species are formed from the nitrogen. Suitable processing parameters for utilization of the apparatus of Fig. 8 include a wafer temperature of from 0°C to 400°C, no rotation of the wafer, a pressure within chamber 222 of from about 5 mTorr to about 15 mTorr (preferably of from about 5 mTorr to about 10 mTorr), and an exposure time of substrate 16 to activated nitrogen species within chamber 222 of from about 5 seconds to about 30 seconds.

Referring next to Fig. 5, substrate 10 is shown at a processing step subsequent to that of Fig. 4, and specifically is shown after exposure to oxidizing conditions. The oxidizing conditions grow an oxide layer 24 from region 14 of substrate 16. The portion of nitrogen-comprising layer 22 previously over region 14 (Fig. 4) is dispersed within oxide 24, and preferably becomes sufficiently dispersed so that the nitrogen does not significantly affect performance characteristics of the oxide in devices incorporating the oxide. Suitable processing forms oxide layer 24 to be

at least about 70Å thick. Such processing is found to adequately distribute nitrogen of the previous layer 22 that had been associated with region 14 so that oxide layer 24 can be incorporated as a gate oxide in transistor devices.

It is noted that nitrogen-comprising layer 22 over oxide 18 of region 12 substantially slows further oxidation of substrate 16 within region 12, and accordingly oxide grows faster over region 14 than over region 12. Thus, oxide 24 is formed to be thicker than the oxide 18 over region 12. Further, nitrogen-comprising layer 22 associated with region 12 remains substantially intact and it can be utilized as, for example, a dopant barrier layer for devices subsequently formed over region 12. In particular aspects of the present invention, the oxidation of wafer 10 forms oxide layer 24 to be at least about 70Å thick, and oxide layer 18 remains less than or equal to about 50Å thick.

Referring to Fig. 6, transistor devices 30 and 32 are formed to be associated with regions 12 and 14, respectively. Devices 30 and 32 comprise oxide layers 18 and 24 as gate oxide, respectively. Device 30 further comprises layers 34, 36 and 38 patterned over oxide 18, and device 32 further comprises layers 40, 42 and 44 patterned over oxide layer 24.

Referring to device 30, layers 34 and 36 can comprise, for example, conductive materials such as, for example, conductively doped silicon and metal silicide, respectively; and layer 38 can comprise, for

example, an insulative cap, such as, for example, a silicon nitride cap. Transistor device 30 can comprise a PMOS device, and conductively doped silicon layer 34 can comprise p-type doped polysilicon. Nitrogen-comprising layer 22 can function as a barrier layer to impede migration of p-type dopant from layer 34 into substrate 16. It is noted that the portion of substrate 16 under oxide layer 18 is an n-type channel for PMOS device 30. Accordingly, if p-type dopant migrates from layer 34 into substrate 16, it can alter dopant concentrations within the n-type channel, and affect or destroy operation of device 30.

Referring to device 32, layers 40, 42 and 44 can comprise, for example, conductively doped silicon, metal silicide, and an insulative cap, respectively. Conductively doped silicon 40 can comprise, for example, n-type doped polysilicon, and metal silicide 42 can comprise, for example, titanium silicide or tungsten silicide. Insulative cap 44 can comprise, for example, a silicon nitride cap. Device 32 corresponds to an NMOS transistor device.

Conductive layers 40 and 42 form a gate for device 32, and conductive layers 34 and 36 form a gate for device 30. Sidewall spacers 46 are shown formed along sidewalls of the gates of devices 30 and 32. Layers 34, 36, 38, 40, 42 and 44, as well as sidewall spacers 46, can be formed by conventional methods.

Lightly doped diffusion regions 48 are shown formed within substrate 16 and proximate a channel region of device 32, and heavily

doped source/drain regions 50 are also shown formed within substrate 16 and associated with device 32. The gate defined by conductive materials 40 and 42 gatedly connects the source/drain regions 50 with one another. Source/drain regions 50 and LDD regions 48 can be formed by conventional methods, and source/drain regions 50 can be heavily doped with n-type conductivity enhancing dopant as is typical for an NMOS device 32.

Lightly doped diffusion regions 52 are shown formed within region 12 of substrate 16 and heavily doped source/drain regions 54 are also shown within region 12 of substrate 16, and shown associated with device 30. A transistor gate defined by conductive layers 34 and 36 gatedly connects source/drain regions 54 with one another. Source/drain regions 54 can be heavily doped with p-type dopant as is typical for a PMOS transistor device 30.

Lightly doped diffusion regions 48 and 52 would typically be lightly doped with n-type conductivity enhancing dopant and p-type conductivity enhancing dopant, respectively. The term "lightly doped" is used to indicate that the diffusion regions 48 and 52 are more lightly doped than are source/drain regions 50 and 54. Typically, source/drain regions 50 and 54 would be doped to a concentration of at least about 10^{19} atoms/cm^3 with conductivity enhancing dopant.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical

features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming an oxide region over a semiconductor substrate, comprising:

forming a nitrogen-containing layer across at least some of the substrate; and

after forming the nitrogen-containing layer, growing an oxide region from the at least some of the substrate, the nitrogen of the nitrogen-containing layer being dispersed within the oxide region.

2. The method of claim 1 wherein the substrate comprises silicon and the oxide region comprises silicon dioxide.

3. The method of claim 1 wherein the substrate comprises monocrystalline silicon and the oxide region is grown from the monocrystalline silicon and comprises silicon dioxide.

4. The method of claim 1 wherein the nitrogen-comprising layer is formed from plasma activated nitrogen species.

5. The method of claim 1 wherein the nitrogen-comprising layer is formed by remote plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 12 inches from the substrate.

6. The method of claim 1 wherein the nitrogen-comprising layer is formed by remote plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 12 inches from the substrate; and wherein the substrate not being biased relative to the plasma during formation of the nitrogen-comprising layer.

7. The method of claim 6 wherein the substrate is maintained at a temperature of from about 550°C to about 1000°C during formation of the nitrogen-comprising layer.

8. The method of claim 6 wherein the substrate is exposed to the nitrogen species for a time of from greater than 0 minutes to about about 5 minutes.

9. The method of claim 1 wherein the nitrogen-comprising layer is formed by plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 4 inches from the substrate.

10. The method of claim 9 wherein the substrate is maintained at a temperature of from about 0°C to about 400°C during formation of the nitrogen-comprising layer.

11. The method of claim 9 wherein the substrate is exposed to the nitrogen species for a time of from greater than 0 seconds to about about 30 seconds.

12. A method of forming a pair of oxide regions over a semiconductor substrate, comprising:

forming a first oxide region which covers only a portion of the substrate;

forming a nitrogen-comprising layer across at least some of the first oxide region and across at least some of the substrate that is not covered by the first oxide region; and

after forming the nitrogen-comprising layer, growing a second oxide region from the at least some of the substrate.

13. The method of claim 12 wherein the first oxide region is formed by:

forming an oxide layer over the covered region and at least some of the uncovered region of the substrate; and

removing the oxide layer from over the uncovered region of the substrate.

14. The method of claim 13 wherein the oxide layer is formed by exposing the substrate to oxidizing conditions.

15. The method of claim 12 wherein the nitrogen-comprising layer is formed by remote plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 12 inches from the substrate.

16. The method of claim 12 wherein the nitrogen-comprising layer is formed by plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 4 inches from the substrate.

17. A method of forming a pair of transistors associated with a semiconductor substrate, comprising:

defining a first region and a second region of the substrate;

forming a first oxide region which covers at least some of the first region of the substrate and which does not cover at least some of the second region of the substrate;

forming a nitrogen-comprising layer across at least some of the first oxide region and across at least some of the uncovered second region of the substrate;

after forming the nitrogen-comprising layer, growing a second oxide region from the uncovered second region of the substrate;

forming a first transistor gate over the first oxide region and a second transistor gate over the second oxide region;

forming first source/drain regions proximate the first transistor gate; and

forming second source/drain regions proximate the second transistor gate.

18. The method of claim 17 wherein the second oxide region is grown to be thicker than the first oxide region.

19. The method of claim 17 wherein the first oxide region is formed by:

forming an oxide layer over the first and second regions of the substrate; and

removing the oxide layer from over the at least some of the second region of the substrate.

20. The method of claim 17 wherein the substrate comprises silicon and the oxide regions comprise silicon dioxide.

21. The method of claim 17 wherein the substrate comprises monocrystalline silicon and the oxide regions comprise silicon dioxide; and wherein the first oxide region is grown from the monocrystalline silicon substrate.

22. The method of claim 17 wherein the nitrogen-comprising layer is formed by remote plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 12 inches from the substrate.

23. The method of claim 17 wherein the nitrogen-comprising layer is formed by plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 4 inches from the substrate.

24. A method of forming a pair of transistors associated with a semiconductor substrate, comprising:

defining a first region and a second region of the substrate, the first region being a p-type doped region and the second region being an n-type doped region;

forming a first oxide region which covers at least some of the first region of the substrate and which does not cover any of the second region of the substrate;

forming a nitrogen-comprising layer across at least some of the first oxide region and across at least some of the second region of the substrate;

after forming the nitrogen-comprising layer, growing a second oxide region from the second region of the substrate;

forming a first transistor gate over the first oxide region and a second transistor gate over the second oxide region;

forming first source/drain regions proximate the first transistor gate to form a PMOS transistor comprising the first transistor gate; and

forming second source/drain regions proximate the second transistor gate to form an NMOS transistor comprising the second transistor gate.

25. The method of claim 24 wherein the PMOS transistor gate comprises p-type doped silicon, and wherein the nitrogen-containing layer formed over the oxide region prevents p-type dopant migration from the doped silicon to the first substrate region.

26. The method of claim 24 wherein the second oxide region is grown to be thicker than the first oxide region.

27. The method of claim 24 wherein the nitrogen-comprising layer is formed by remote plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 12 inches from the substrate.

28. The method of claim 24 wherein the nitrogen-comprising layer is formed by plasma nitridation utilizing nitrogen species generated in a plasma that is at least about 4 inches from the substrate.

ABSTRACT OF THE DISCLOSURE

The invention encompasses a method of forming an oxide region over a semiconductor substrate. A nitrogen-containing layer is formed across at least some of the substrate. After the nitrogen-containing layer is formed, an oxide region is grown from at least some of the substrate. The nitrogen of the nitrogen-containing layer is dispersed within the oxide region. The invention also encompasses a method of forming a pair of transistors associated with a semiconductor substrate. A substrate is provided. A first region of the substrate is defined, and additionally a second region of the substrate is defined. A first oxide region is formed which covers at least some of the first region of the substrate, and which does not cover any of the second region of the substrate. A nitrogen-comprising layer is formed across at least some of the first oxide region and across at least some of the second region of the substrate. After the nitrogen-comprising layer is formed, a second oxide region is grown from the second region of the substrate. A first transistor gate is formed over the first oxide region, and a second transistor gate is formed over the second oxide region.

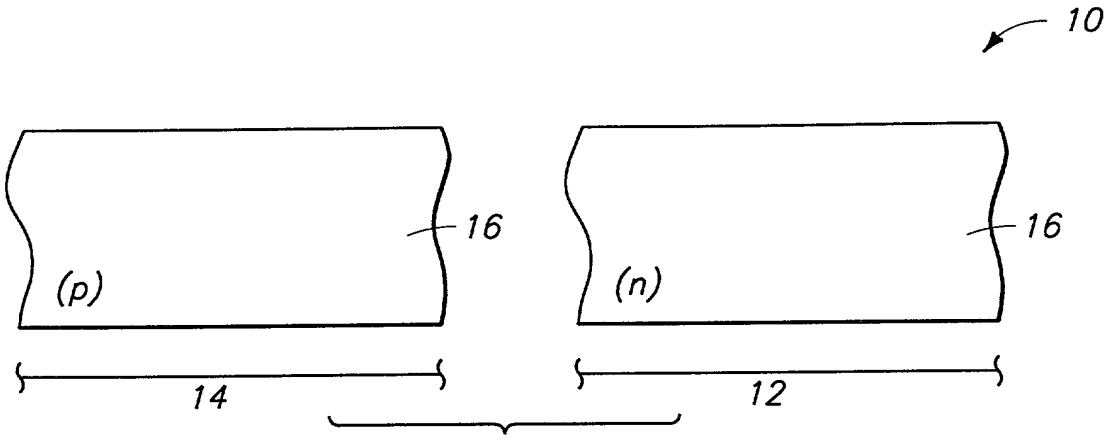

Fig. 1

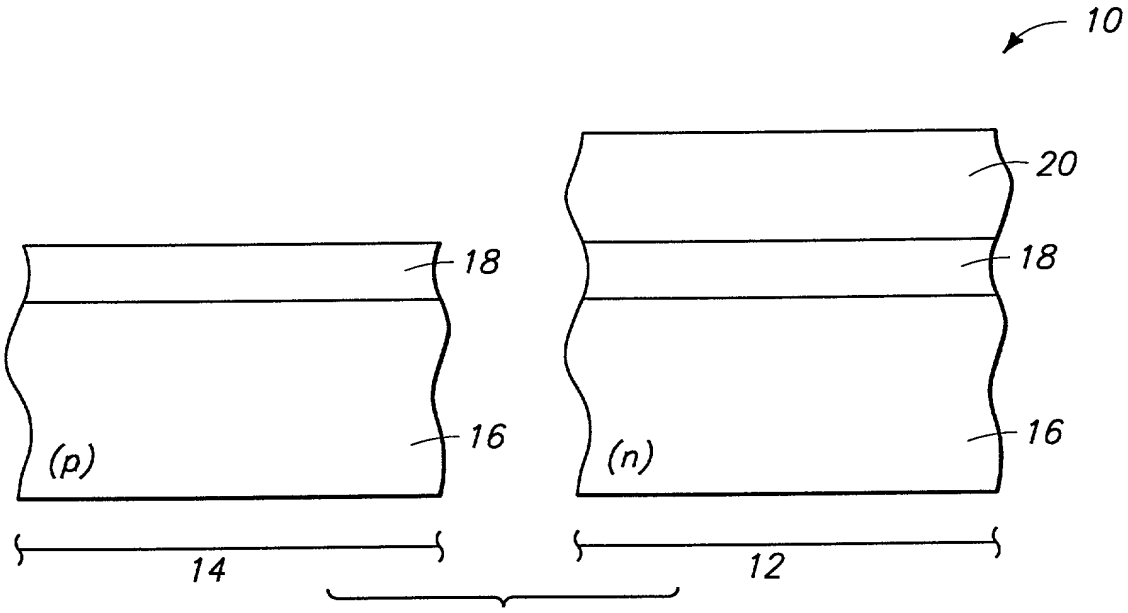

Fig. 2

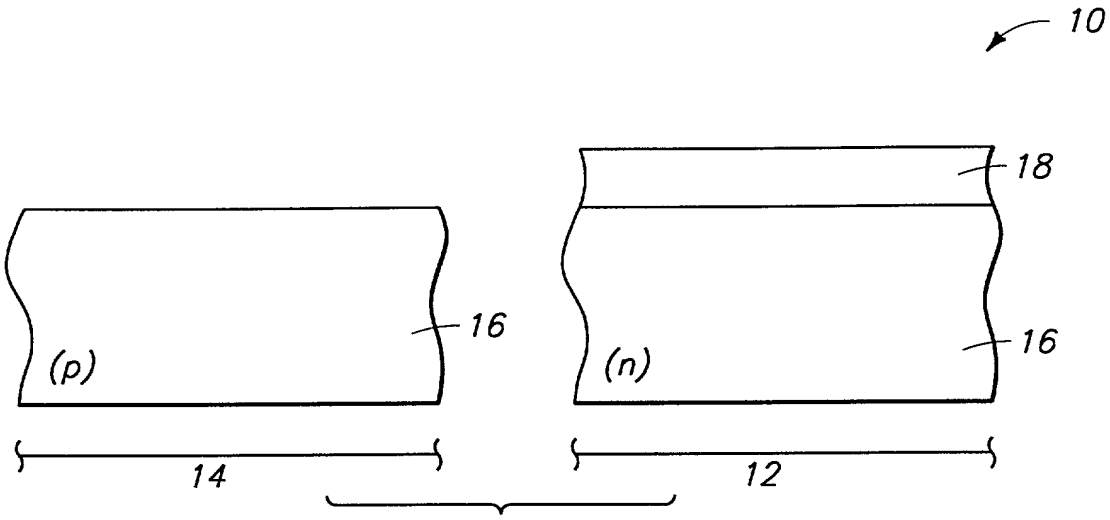

Fig 3

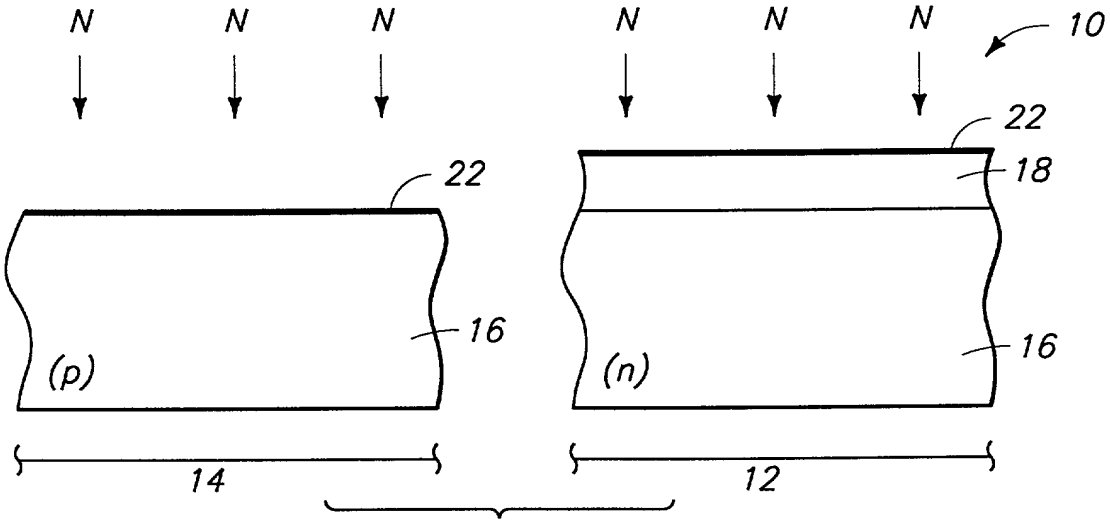

Fig 4

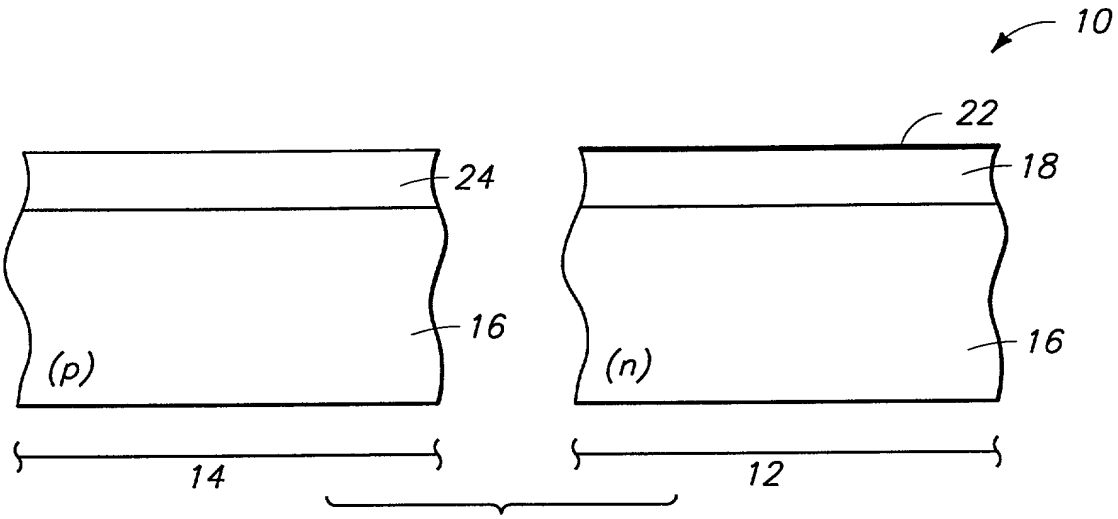
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Fig 5

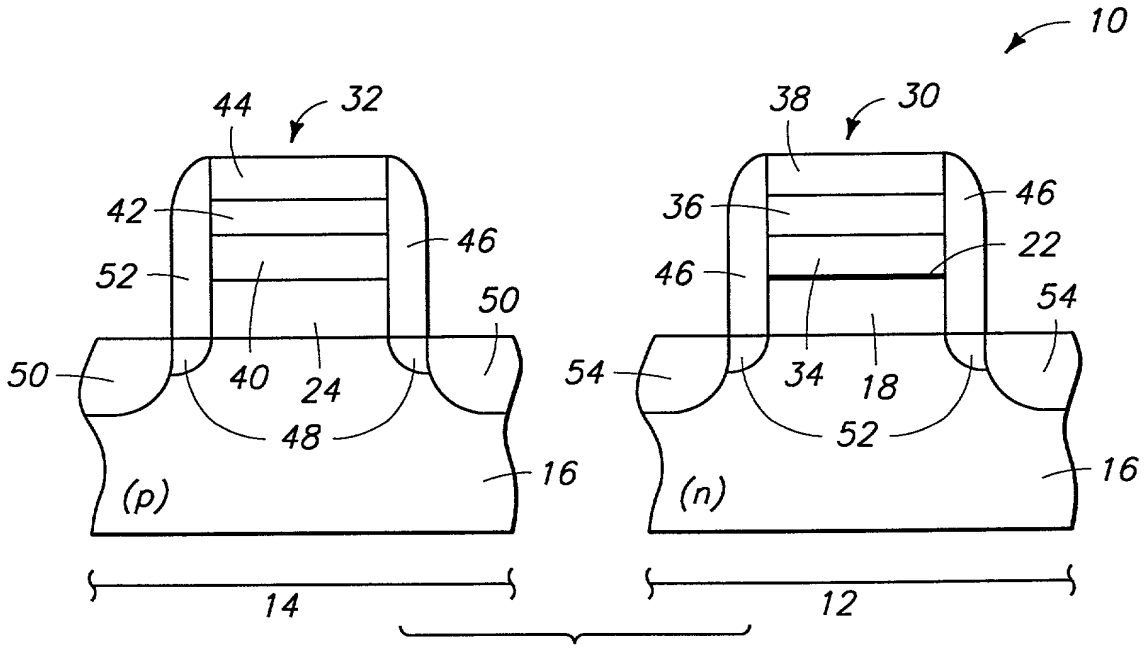
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Fig 6

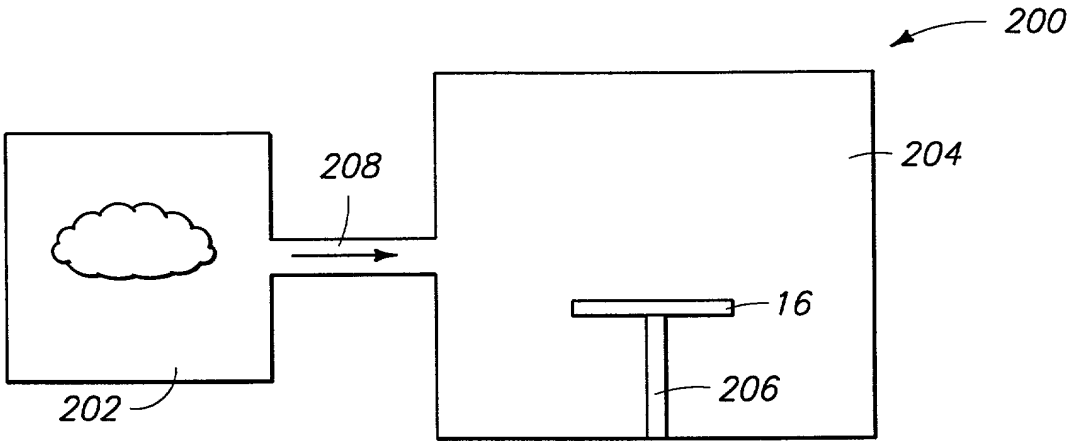

Fig. 7

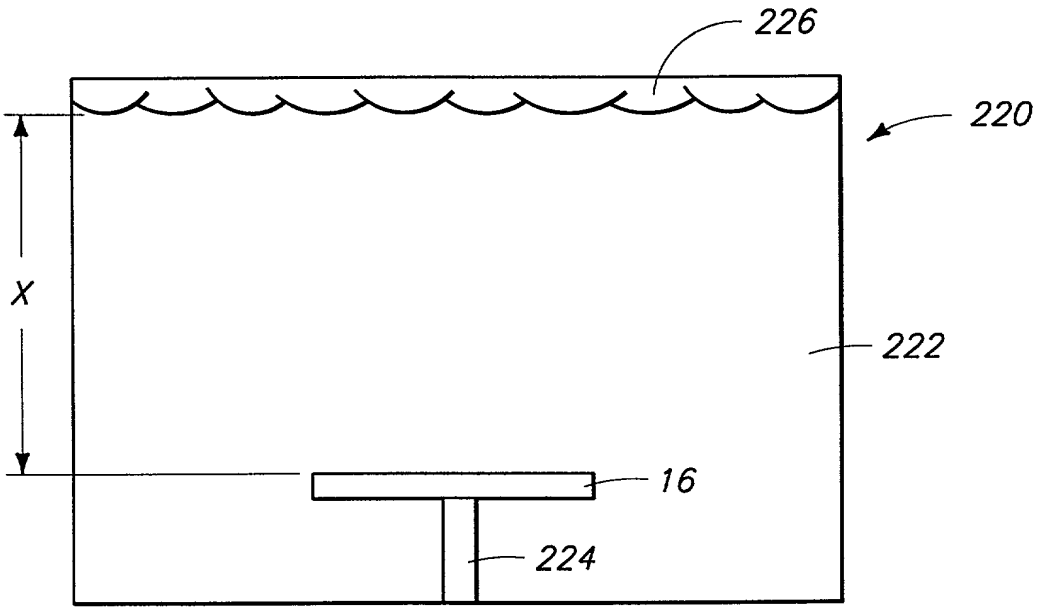

Fig. 8

DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Forming Oxide Regions Over Semiconductor Substrates, and Methods of Forming Transistors Associated With Semiconductor Substrates, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were

made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

Full name of sole inventor: **John T. Moore**

Inventor's Signature: John T. Moore

Date: 6/14/00

Residence: **Boise, ID**

Citizenship: **US**

Post Office Address: **12530 W. Lexus Ct.**
Boise, ID 83713

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. ..... Filed herewith
Filing Date ..... Filed herewith
Inventor ..... John T. Moore
Assignee ..... Micron Technology, Inc
Group Art Unit ..... Unknown
Examiner ..... Unknown
Attorney's Docket No. MI22-1384
Title: Methods of Forming Oxide Regions Over Semiconductor Substrates, and Methods of Forming Transistors Associated With Semiconductor Substrates

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR §3.73(b)

To: Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., the Assignee of the entire right, title and interest in the above-identified patent application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., listed as follows:

David P. Roberts	Reg. No. 23,032
Randy A. Gregory	Reg. No. 30,386
Mark S. Matkin	Reg. No. 32,268
James L. Price	Reg. No. 27,376
Deepak Malhotra	Reg. No. 33,560
Mark W. Hendricksen	Reg. No. 32,356
David G. Latwesen	Reg. No. 38,533
George G. Grigel	Reg. No. 31,166
Keith D. Grzelak	Reg. No. 37,144
James D. Shaurette	Reg. No. 39,833
Frederick M. Fliegel	Reg. No. 36,138
Donald Brent Kenady	Reg. No. 40,045

James E. Lake Reg. No. 44,854
Bernard Berman Reg. No. 37,279

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia Pappas Dennison (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

The Assignee certifies that the above-identified Assignment has been reviewed and to the best of Assignee's knowledge and belief, title is in the Assignee, and a copy of the Assignment is submitted herewith.

Please direct all correspondence regarding this application to:

Customer No. 021567
Wells, St. John, Roberts, Gregory & Matkin P.S.
Attn: David G. Latwesen, Ph.D.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Telephone: (509) 624-4276
Facsimile: (509) 838-3424

MICRON TECHNOLOGY, INC.

Dated: 6-16-00 By: _____

Name: Michael L. Lynch, Esq.
Title: Chief Patent Counsel

Attachment: Copy of Assignment; Copy of Board of Directors' Resolution

MICRON TECHNOLOGY, INC.
BOARD OF DIRECTORS RESOLUTIONS

WHEREAS, certain key employees require the authority to execute certain documents on behalf of the Company in order to enable them to effectively and efficiently carry out their responsibilities and duties to the Company.

NOW THEREFORE BE IT RESOLVED, that the Board hereby approves and authorizes Mr. Michael L. Lynch, Assistant General Counsel for Intellectual Property, to execute on behalf of the Company, documents pertaining to the Company's patent prosecution matters, including but not limited to documents relating to representation before a patent examining authority, patent terms and other patent prosecution procedures, both in the United States and other countries, upon such terms and conditions as the General Counsel of the Company shall deem necessary or appropriate.

MICRON TECHNOLOGY, INC.
CERTIFIED COPY OF RESOLUTIONS

I, Jan R. Reimer, the Assistant Secretary of Micron Technology, Inc. do hereby certify, that the resolutions attached hereto represent a complete, true and correct copy of the resolutions duly adopted by the Board of Directors of Micron Technology, Inc., a corporation duly organized and existing under the laws of the State of Delaware, at a meeting duly held on March 25, 1996, a quorum being present, and have been entered into the minutes of said meeting; that I am the keeper of the corporate seal and of the minutes and records of this Corporation; and that the said resolutions have not been rescinded or modified.

The resolutions attached hereto are in conformity with the Articles of Incorporation and Bylaws of the Corporation and are now in full force and effect.

I further certify that the person whose name and signature is set out below is the person authorized to act for said corporation in transactions with and pursuant to the foregoing resolutions, and that such person is now duly qualified and acting in his respective capacity:

NAME AND TITLE	SIGNATURE
Michael L. Lynch, Assistant General Counsel for Intellectual Property	

IN WITNESS WHEREOF, I have hereunto subscribed my name and affixed the seal of the said corporation, this 6th day of May, 1996.

Jan R. Reimer, Assistant Secretary

(SEAL)